Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Z**
2. **OUT**
3. **–VS**
4. **X1**
5. **X2**
6. **GND**
7. **VOS**
8. **Y2**
9. **Y1**
10. **+VS**

**.092”**

**CIC01382**



**MASK**

**REF**

**8**

**7**

**1**

**2**

**3**

**4**

**5 6**

**10 9**

**.105”**

**DRAFT**

**UNSURE OF PIN ASSIGNMENTS**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005” X .005”**

**Backside Potential:**

**Mask Ref: CIC01382**

**APPROVED BY: DK DIE SIZE .092” X .105” DATE: 4/11/18**

**MFG: T.I. / BURR BROWN THICKNESS .021” P/N: AD532**

**DG 10.1.2**

#### Rev B, 7/1